Remarks

Claims 1-17 are pending in the present application. Claims 1, 10 and 17 are objected to due to alleged informalities. Claim 6 stands rejected under 35 U.S.C. § 112 as being indefinite. Claims 1-6, 10, 11, 15, and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mueller et al. (4,631,495). Claims 7-9, 12-14, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mueller et al taken alone. In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Objections

Claims 1, 10 and 17 stand objected to for the inclusion of a comma (",") after the word "and." The manner in which Applicant choose to punctuate claims 1, 10 and 17 is entirely within the Applicant's discretion, and should not provide any basis for the above-referenced claim objections. The placement of the commas in claims 1, 10 and 17 does not make the claims grammatically, phonetically or typographically incorrect, and is entirely proper. Hence, reconsideration and withdrawal of this objection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 112

Claim 6 is rejected under 35 U.S.C. § 112, Second Paragraph, as being "indefinite." Particularly, the Examiner contends that it is still not clear how "at least one transistor" can comprise a "number of transistors." Claim 6 was previously amended to specify that the "at least one first transistor" recited in claim 1 comprises a "specific number of transistors selected to provide an optimum noise characteristic" (See, Amendment Under 37 C.F.R. § 1.115, dated April 29, 2005). It is a well-established tenet of claim interpretation that the modifier "at least one..." means 'one or more' of the specified element. Thus, in reciting "at least one first transistor" claim 1 specifies one or more transistors (e.g., 1, 2, 3, etc.). Claim 6 further modifies claim 1 to specify that the particular number of transistors are selected to provide an "optimum noise characteristic." So, for example, claim 1 specifies any number of transistors from one to infinity, but the specific number of transistors (e.g., 4 transistors) is selected to provide the optimum noise characteristic. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-6, 10, 11, 15, and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Mueller et al. (4,631,495). For the reasons set forth in detail below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claim 1 recites:

> A multi-stage amplifier comprising: a first amplifier stage including at least one first transistor, said at least one first transistor selected to provide an optimum noise characteristic; and, a second amplifier stage including at least one second transistor, said at least one second transistor selected to provide an optimum gain characteristic, wherein optimum noise characteristic is provided by selecting an appropriate geometry for the at least one first transistor. [emphasis added].

Thus, claim 1 requires a multi-stage amplifier including a "first stage" with an amplifier selected to provide an "optimum noise characteristic", and a "second stage" with an amplifier selected to provide an "optimum gain characteristic," such that the optimum noise characteristic is provided by "selecting an appropriate geometry" for one or more transistors. As discussed below, Mueller fails to disclose, teach or suggest such an invention.

Mueller teaches a low noise preamplifier circuit which includes a low noise input stage 12, and gain stages 14-1, 14-2 (See Fig. 2). In one exemplary embodiment, the low noise input stage includes bipolar junction transistors (BJTs) 20-1, 20-2, diodes 24-1, 24-2, coupling capacitor 23, DC blocking capacitors 21-1, 21-2, bias resistors 26-1, 26-2, tuning capacitance 28, damping resistance 30, load inductance 27, and capacitor 32. The overall impedance of the low noise input stage 12 is adjusted so as to provide the lowest possible noise figure F_1 (see, col. 4, lines 46-51).

Nowhere does Mueller disclose, teach or suggest altering the geometry of the BJTs 20-1, 20-2 to achieve an "optimum noise characteristic." By contrast, Mueller teaches (if anything) altering the impedance values of all the surrounding circuit elements (e.g., coupling capacitor 23, DC blocking capacitors 21-1, 21-2, etc.) to achieve the proper noise figure. Specifically, Mueller discusses "individually adjusting the flow of current in the device controlled-conduction circuit, i.e., the collector-emitter circuit of each bipolar junction transistor" to control the noise figure for each BJT (see, col. 8, lines 15-20). Mueller also suggests that the BJTs 20-1, 20-2 may comprise commercially available transistors with specific, unchangeable geometries (e.g., Microwave Associates MA42197, Motorola MRF904; see col. 6, line 67 – col. 7, line3). Thus, it is clear that Mueller does not teach or suggest transistors with geometries selected to provide an "optimum noise characteristic," as particularly recited in claim 1.

As noted above, Mueller does not disclose, teach or suggest a multi-stage amplifier including at least one transistor whose geometry is selected to provide an "optimum noise characteristic." Hence, reconsideration and withdrawal of this ground of rejection with respect to claim 1, and claims 2-9 dependent thereon, is respectfully requested.

Independent claim 10 recites similar limitations to those discussed above with reference to independent claim 1. In particular, claim 10 recites a method whereby the geometry of one or more transistors are selected based on an "optimum noise" characteristic. Accordingly, for those reasons discussed above with reference to independent claim 1, reconsideration and withdrawal of this rejection with respect to claims 10, 11 , 15 and 16 is also respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 7-9, 12-14, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller et al. For the reasons set forth in detail below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claims 7 and 12 have been canceled by this Amendment, and claims 8, 9 13 and 14 are all dependent upon independent claims 1 and 10 discussed above. Accordingly, claims 8, 9 13 and 14 should be considered allowable for at least those same reasons advanced above for the allowance of claims 1 and 10.

Further, the Examiner has pointed to no teaching or suggestion in Mueller (or any other reference) that an "optimum noise characteristic" can be provided for in an amplifier stage by "selecting and appropriate geometry" for at least one transistor of the amplifier stage (as previously recited in claims 7 and 12, and as now recited in claims 1 and 10).

To establish a prima facie case of obviousness, three basic criteria must be met: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, M.P.E.P. 2142 (Eighth Edition, Feb. 2003).

As a threshold matter, there must be some teaching, suggestion or motivation in the prior art to make the specific change made by the applicant. In re Dance, 160 F.3d 1339, 1343 (Fed. Cir. 1998). Obviousness should be measured "at the time the invention was made" (i.e. the filing date of the application), and with no prior knowledge of the applicant's disclosure. In re Dembiczak, 175 F.3d 994, 998-999 (Fed. Cir. 1999).

Obviousness cannot be established by hindsight combination to produce the claimed invention. In re Dance, 160 F.3d. at 1343. The Examiner must show reasons why the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the prior art references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

Since there is clearly no teaching or suggestion in the prior art to modify the geometry of the transistors in the low noise input stage 12 of Mueller (e.g., 20-1, 20-2), prompt allowance of claims 1 and 10 is earnestly solicited.

Independent claim 17 recites a method for producing a multi-stage amplifier by selecting one or more transistors "such that at least one noise circle and at least one gain circle intersect at or near the center of a corresponding Smith Chart" for the amplifier. Mueller fails to disclose, teach or suggest such an invention. In fact, Mueller nowhere discusses the analyzing of Smith Charts as a tool for setting the noise and gain characteristics of an amplifier. For this reason alone, the Applicant submits that the rejection of claim 17 should be withdrawn.

Additionally, independent claim 17 recites similar limitations to those discussed above with reference to independent claims 1 and 10. In particular, claim 17 recites a method whereby transistors are selected based on "optimum noise" and "optimum gain" characteristics, such that the optimum gain characteristic is provided by selecting an "appropriate geometry" for one or more transistors. Accordingly, for those reasons discussed above with reference to independent claim 1, reconsideration and withdrawal of this rejection with respect to claim 17 is also respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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